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APPLICATION NO. FILING DATE		FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/624,699	07/22/2003	lain Robertson	TI-32313	7070		
• 23494	7590 10/31/2006		EXAMINER			
	STRUMENTS INCORPOR	TRAN, KHAI				
DALLAS, T	5474, M/S 3999 CX 75265		ART UNIT PAPER NUM			
			2611			
			DATE MAILED: 10/31/2006			

Please find below and/or attached an Office communication concerning this application or proceeding.

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			Application No.		Applicant(s)			
Office Action Occurrence		10/624,699		ROBERTSON ET AL.				
Office Action Summary			Examiner		Art Unit	-		
		KHAI TRAN		2611				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply								
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).								
Status								
1)⊠ Re	esponsive to communication(s) file	ed on <i>21 .lu</i>	lv 2003					
·	Responsive to communication(s) filed on <u>21 July 2003</u> . This action is FINAL . 2b)⊠ This action is non-final.							
/=	nce this application is in condition	<i>'</i> —		l matters, pro:	secution as to the	e merits is		
<i>,</i> —	sed in accordance with the practic		•	•				
Disposition	of Claims							
4)⊠ Cla	aim(s) <u>1-28</u> is/are pending in the a	application.						
•	4a) Of the above claim(s) is/are withdrawn from consideration.							
	5) Claim(s) is/are allowed.							
6)⊠ Cla	6)⊠ Claim(s) <u>1,5-7,19 and 23-25</u> is/are rejected.							
7)⊠ Cla	7)⊠ Claim(s) <u>2-4,8-18,20-22 and 26-28</u> is/are objected to.							
8) <u></u> Cla	aim(s) are subject to restric	tion and/or	election requirement	nt.				
Application	Papers							
9)∐ The	e specification is objected to by the	e Examiner						
10)∐ The	e drawing(s) filed on is/are:	a) acce	epted or b) dobject	ed to by the E	xaminer.			
Ар	plicant may not request that any object	ction to the c	Irawing(s) be held in a	beyance. See	37 CFR 1.85(a).			
Re	placement drawing sheet(s) including	the correcti	on is required if the dr	awing(s) is obj	ected to. See 37 C	FR 1.121(d).		
11)∐ The	e oath or declaration is objected to	by the Exa	aminer. Note the att	ached Office	Action or form P	ΓΟ-152.		
Priority und	er 35 U.S.C. § 119							
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a)⊠ All b)□ Some * c)□ None of:								
_	1. Certified copies of the priority documents have been received.							
_	2. Certified copies of the priority documents have been received in Application No							
J. _L	3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).							
* See the attached detailed Office action for a list of the certified copies not received.								
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Attachment(s)								
	References Cited (PTO-892)			rview Summary (
	Draftsperson's Patent Drawing Review (Pon Disclosure Statement(s) (PTO/SB/08)		er No(s)/Mail Da ice of Informal Pa					
	(s)/Mail Date <u>8/2/2006</u> .		6) 🔲 Oth		· •			

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DETAILED ACTION

Drawings

1. Figures 1-5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. Claims 5-7, 23-25 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 5, line 4, the term "the phase of **the or** a master one" is not clear.

Claims 6-7 are rejected by virtue of their dependency.

Regarding claim 23, line 3, the term "to a, or the" is not clear.

Claims 24-25 are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 4. Claims 1, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Kikuchi et al (U.S. Pat. 6,018,305).

Regarding claim 1, Kikuchi et al disclose a circuit as shown in Figures 1-2, comprising: a plurality of data input terminals each for receiving respective serial data signals having the same bit rate (s serial to parallel converters 57, 57(1) to 57(m), receiving serial data signals); bit clock generating means (clock signal CLK1) responsive bit clock signal aligned to provide for each a respective bit clock signal aligned with that data signal (from serial DATA input SD) and having a period equal to twice the bit period of the data signal; bit clock phase adjustment means responsive to the relative phases of the bit clocks to adjust the phases of the bit clocks relative to one another so that they all lie within a common interval of 180° of phase, where 360° of phase represents the period of the bit clock (see abstract, The serial to parallel conversion apparatus includes a first divider for dividing a first clock signal into 2 to produce a second clock signal and adjusting the phase of the second signal in accordance with a first phase adjustment signal, a first serial to parallel converter for converting serial data into parallel data of 2 bits in response to the second clock signal, a pair of shift registers for receiving and storing the different bits of the parallel data and successively shifting the stored bits in response to the second clock signal, a second divider for dividing the second clock signal into 4 to produce a third clock signal, a second detector for producing the first phase adjustment signal and the second phase

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adjustment signal based on the stored data of the shift registers, and a pair of second serial to parallel converters for receiving the different bits of the parallel data and each producing first parallel data of 4 bits in response to the third clock signal).

Claim 19 is similar to claim 1. Therefore, claim 19 is rejected under a similar rationale.

Allowable Subject Matter

- 5. Claims 2-4, 8-18, 20-22, 26-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 6. Claims 5-7, 23-25 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.
- 7. The following is a statement of reasons for the indication of allowable subject matter: Kikuchi et al fail to disclose a circuit and method for receiving a plurality of parallel data signals of the same bit rate comprising: wherein the plurality of bit clocks comprise a master one, the others of the plurality being slave ones, and the bit clock phase adjustment means is arranged to compare the master bit clock signal with the phase of the other or each of the other, slave, bit clock signals and to adjust the phase of the or each slave bit clock signal if it falls outside the common interval of 180° of phase as recited claims 2-20; wherein the phase adjustment means is arranged to adjust the phase of a bit clock signal that is outside the common interval to a phase that

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is defined with respect to the phase of the or a master one of the bit clock signals and that is within the common interval as recited in claims 5, 23.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pickering et al (U.S. Pat. 7,035,368) disclose a high speed parallel link receiver.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHAI TRAN whose telephone number is (571) 272-3019. The examiner can normally be reached on 7:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JAY PATEL can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Womawangtu KHAI TRAN

Primary Examiner Art Unit 2611

KT October 27, 2006